



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 4350  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,887	08/20/2001	Shinji Shiraga	35.C15684	4036

5514 7590 04/17/2006

FITZPATRICK CELLA HARPER & SCINTO  
30 ROCKEFELLER PLAZA  
NEW YORK, NY 10112

EXAMINER

SURYAWANSHI, SURESH

ART UNIT PAPER NUMBER

2115

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/931,887

Applicant(s)

SHIRAGA ET AL.

Examiner

Suresh K. Suryawanshi

Art Unit

2115

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 2/6/06 RCE.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 28-55 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 50-55 is/are allowed.
- 6) ☒ Claim(s) 28-49 is/are rejected.
- 7) ☒ Claim(s) 29 and 40 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. Claims 28-55 are presented for examination.

#### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 28-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haroun et al (US Patent 6,151,262; hereinafter Haroun).
4. As per claims 1, 33, 39, and 44, Haroun clearly discloses an invention concerning power consumption control of memory having a fully powered state and a lower power state. The invention changes the memory to the fully powered state upon receipt of a memory access request. The memory is returned to a lower power state after expiration of a grace period following a last memory access request [col. 2, lines 15-30; col. 3, lines 43-57; col. 10, lines 1-13]. The mode setting means is enabled through a control register [col. 4, lines 30-41; col. 5, lines 44-62]. The memory is set to the power saving mode while the mode setting means is in the enabled state [Fig. 6; col. 7, line 43 -- col. 8, line 8; Note in fig. 6 when c is equal to C1, last memory access, then the memory is set into ACTIVE 403 state (i.e., enabled state). Upon a delay of T4, the memory is put into a power saving mode].

Art Unit: 2115

Haroun does not expressly disclose that the memory access was a read of a power saving mode transfer instruction from the memory for setting the processing means to a power saving mode. However, Haroun does not limit the invention for some specific instructions access from the memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention for a power saving mode transfer instruction by the processing means from the memory. Moreover, Haroun discloses that the predetermined number of memory access request can be fixed in manufacture time [col. 10, lines 35-37]. Thus, the invention could be tailored for the power saving mode transfer instruction access from the memory.

5. As per claim 30, Haroun discloses that said processing means detects an interruption for returning to the normal operation mode from the power saving mode [col. 2, lines 17-18; col. 10, lines 2-9; fully powered state upon receipt of a memory access request].

6. As per claim 31, Haroun discloses that said processing means outputs the information for notifying said mode setting means that said processing means is transferred to power saving mode [a read of a power saving mode transfer instruction from the memory].

7. As per claim 32, 38, 43 and 49, Haroun discloses that said mode setting means sets the memory to the power saving mode after an end of memory transfer in progress [col. 2, lines 15-30; col. 3, lines 43-57; col. 10, lines 1-13].

Art Unit: 2115

8. As per claims 34 and 45, Haroun discloses that said mode transfer means supplies the memory with a predetermined signal to transfer the memory to the power saving mode from a normal operation mode [col. 2, lines 15-30; col. 3, lines 42-57].

9. As per claim 35, Haroun discloses that said mode transfer means transfers the memory to a normal operation mode in accordance with an interruption for returning said processing means to a normal operation mode from the power saving mode [col. 2, lines 17-18; col. 10, lines 2-9; fully powered state upon receipt of a memory access request].

10. As per claims 36 and 47, Haroun discloses that said processing means sets a time of period of the waiting state [col. 2, lines 15-30; col. 3, lines 43-57; col. 10, lines 1-13; grace period].

11. As per claims 37 and 48, Haroun discloses that said processing means instructs said mode transfer means to start counting a lapse of a time period of the waiting state [Fig. 6; col. 2, lines 15-30; col. 3, lines 43-57; col. 10, lines 1-13; a grace period].

12. As per claims 41 and 46, Haroun discloses a returning step of returning the processor and the memory to a normal operation mode from the power saving mode [col. 2, lines 15-30; col. 3, lines 42-57].

Art Unit: 2115

13. As per claim 42, Haroun discloses an outputting step of outputting the information for notifying memory controller that the processor is transferred to the power saving mode [a read of a power saving mode transfer instruction from the memory], and wherein the memory is set to the power saving mode at said power saving mode setting step in accordance with the information outputted at said outputting step while said mode setting means is in the enabling state [Fig. 6; col. 7, line 43 -- col. 8, line 8; Note in fig. 6 when c is equal to C1, last memory access, then the memory is set into ACTIVE 403 state (i.e., enabled state). Upon a delay of T4, the memory is put into a power saving mode].

***Allowable Subject Matter***

14. Claims 29 and 40 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. Claims 50-55 are allowed.

***Response to Arguments***

16. Applicant's arguments with respect to claims 28-49 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2115

*Conclusion*

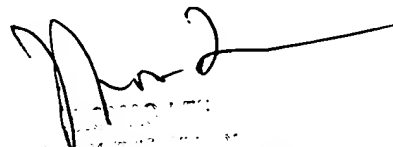
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks

April 12, 2006



Suresh K. Suryawanshi  
Examiner  
Art Unit 2115